THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AKIHIKO KOH, TSUTOMU SAMPEI, NOBUHISA WATANABE, and AKIHIRO KIKUCHI

Appeal 2006-2407
Application 09/802,857
Technology Center 2100

Decided: June 21, 2007

Before JAMES D. THOMAS, JOSEPH F. RUGGIERO, and MAHSHID D. SAADAT, *Administrative Patent Judges.*

THOMAS, *Administrative Patent Judge.*

ON REQUEST FOR REHEARING

In a Decision mailed October 31, 2006, we affirmed the Examiner's rejection of all claims on appeal under 35 U.S.C. § 103. On December 29,

2006, Appellants filed a Request for Rehearing of this Decision. The above-noted panel only recently received this Request for Rehearing.

The Request repeatedly urges that the prior art references to Sagane and Hosotani fail to teach or suggest or otherwise indicate that the respective CPUs in these references effectively receive the plurality of coincidence signals claimed in representative independent claim 13 on appeal. This argument is reflective of the actual language of claim 13 that requires "a central processing unit receiving said plurality of coincidence signals."

At the outset, we reproduce below the discussion from Specification page 25, lines 1 through 14 upon which the feature of a plurality of coincidence signals is based:

> [T]he output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 can be input to the CPU 10 as two different interrupt request signals. Accordingly, the CPU 10 receives these as different interrupt requests and executes the debugged programs separately to correct the two bugs. In general, however, the number of the interruptions that the CPU 10 is able to process is limited, so a plurality of bug processings have to be assigned to a single interruption. In this case, as shown in Fig. 7, the output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 are input to an AND gate 130, and the output signal S_A of the AND gate 130 is input to the CPU 10 as the interrupt request signal.

This portion makes clear that, from the showing in Figure 7, the coincidence detecting circuits 120-1 and 120-2 provide separate coincidence or compare signals S_{A1} and S_{A2}, both of which feed a single AND circuit 130 which outputs a signal S_A. The discussion indicates that these coincidence detecting circuits output two different interrupt request signals from which the "CPU 10 receives these as different interrupt requests." The latter portion of the discussion indicates that only one interrupt request

signal is submitted to the CPU at a given time. Thus, the plurality of coincidence signals recited near the end of independent claim 13 on appeal is perhaps somewhat misdescriptive because the CPU is not stated as disclosed to receive a plurality of the coincidence signals at the same time. This was discussed in the paragraph bridging pages 5 and 6 of our original opinion.

Moreover, it is thus clear that the claimed plural generated coincidence signals are not directly inputted to the CPU as the actual claimed recitation seems to indicate. It is also significant to realize that any coincidence signal that is received is treated "as" an interrupt signal as disclosed.

We have and continue to consider the applied prior art to Sagane and Hosotani from an artisan's perspective. Both references teach common bus environments associated with respective CPUs. The emphasis of our prior decision was to show the analogue of the showing of Sagane's Figure 3 embodiment to that which is shown in his Figure 1 embodidment, an approach also followed by the Examiner. The coincidence signal E outputted from the comparator 8 in the Figure 1 embodiment feeds the interrupt control circuit 7d which in turn directly feeds the bottom right corner of the CPU 2 with an interrupt signal. The artisan clearly would have understood that this interrupt signal *per se* is a type of coincidence signal since it is the result of the compare operation and is characterized as such as signal E.

As stated at the bottom of page 7 of our prior decision, we agreed with the Examiner's remarks at pages 4 through 6 of the Answer that the mere reception of coincidence signals by the CPU of claim 13 does not

require explicitly a direct connection or a direct coupling. From an artisan's perspective, the artisan would consider the interrupt signal actually received by the CPU 12 as a kind of coincidence signal.

As our prior decision clarified as to the Examiner's approach, Sagane's Figure 3 embodiment does not use *per se* an interrupt control circuit 7d like the showing in Figure 1. In an analogous manner, the signal A from a corresponding comparator 8 is inputted to the switch 23 which in turn indirectly feeds the data bus 5 which in turn feeds the CPU 2 with what amounts to, as we explained in our prior decision, an interrupt-type signal utilizing a different approach. The Examiner relied upon a teaching at column 2, lines 6 through 14 as indicating that the output of this access switching means switched access by the processing means from the fixed storage means to the correction content storage means, and the control means. This showing in Figure 3 and the flowchart functionality in Figure 4 of its operation which is discussed at pertinent portions beginning at column 6, line 41 makes it clear that the CPU functions to effectively "receive" signals comparable to an interrupt type signal according to the Figure 1 embodiment such as to cause the CPU to change processing sources and to execute a correction program in RAM.

The bulk of our discussion in the prior opinion focused upon an artisan's perspective of what the artisan would appreciate from the showing in Figure 3 and not that in Figure 1. These remarks here make it clear that, from an artisan's perspective, the CPU 2 in Sagane receives, in effect, one or a plurality of time sequenced coincidence/interrupt type signals.

The remarks beginning at page 11 of the Request for Rehearing as to Hosotani are equally misplaced. This reference also operates in a common

bus environment for central processing units, an approach well known in the data processing arts. We briefly discussed this supporting reference at page 8 of our prior opinion. The artisan would have well appreciated that the output of the OR gate 14 is selectively switched by the connection control 10 which controls operability of various circuits which indirectly feed signals to the data bus 5 which in turn directly feeds the CPU 1.

Appellants recognize in their discussion at pages 12 and 13 of the Request for Rehearing that the claims do not require a direct connection of the claimed coincidence signals to the CPU which we discussed, as noted earlier, at the bottom of page 7 of the original opinion. Thus, the claim must be read to implicitly permit/require an indirect reception of such signals. As consistent with the Examiner's position that the claim does not require the plurality coincidence signals themselves to be received by the central processing unit, we do not agree with Appellants' urgings since Appellants have agreed that the mere reception of coincidence signals by the CPU of claim 13 does not require explicitly a direct connection or a direct coupling of them. The prior decision does in fact show such an indirect (through various intermediate circuits) reception in both Sagane and Hosotani. The characterization of the signals actually received by the respective references directly or indirectly notwithstanding, the artisan would clearly understand the functionality of the applied prior art as consistent within 35 U.S.C. § 103 of the subject matter recited in the argued claim 13 on appeal.

In view of the foregoing, we have considered in detail Appellants' Request for Rehearing of our prior Decision, but are not persuaded by the Request to make any changes therein.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

DENIED

tdl

Rader Fishman & Grauer PLLC
Lion Building
1233 20th Street N.W., Suite 501
Washington DC 20036